International Journal of Research in Advent Technology, Vol.6, No.6, June 2018
E-ISSN: 2321-9637
Available online at www.ijrat.org

Modified Transistor Clamped H-bridge-based Cascaded Multilevel inverter with high reliability.

Soujanya Kulkarni (PG Scholar) [1], Sanjeev Kumar R A (Asst.Professor) [2]
Department of Electrical and Electronics[1, 2], *PDA college of Engineering Kalaburgi* [1, 2]
Email:Soujanya.s.v.k@gmail.com[1], *sanju.san999@gmail.com*[2]

Abstract-: The rising of the voltage above the voltage limits of classical two-level inverter is supplied through a Multilevel Inverter. Less Total Harmonic Distortion, low voltage stress across the switch, low dv/dt stress are the main causes of widespread application of multilevel inverters (MLIs). The semiconductor devices are the most delicate parts which result in low reliability of MLI as compared to two level inverters. Hence, fault tolerance is one of the major concerns in many industrial applications where continuity is utmost important, to achieve continuity in supply certain modification has been accomplished, in order to increase the redundancy and hence the Reliability of Transistor Clamped H-Bridge based cascaded MLI. In the classical TCHB inverter, if any switch is subjected to fault then the conversion operation is halted until the faulted switch is replaced. This paper presents study of modified Transistor Clamped H-Bridge (TCHB) Multilevel Inverter. The proposed topology consists of two legs of H-bridge, one bidirectional switch and it is powered by DC source. The gating pulses can be generated by using Multi-Carrier Pulse Width Modulation (MCPWM). The Total Harmonic Distortion (THD) value is obtained by using FFT analysis, the THD values for Phase Disposition MCPWM. The modeling and the analysis of the work can be performed on MATLAB software based Simulation on SIMULINK platform for single phase five level transistor Clamped H-Bridge inverter.

Index Terms- TCHB, fault tolerance, THD, Multi Carrier Pulse width Modulation.

1. INTRODUCTION

The Use of multilevel converter has been continuously increasing over the last years. Traditionally, these converters were used in high-power and medium-voltage applications. The usage of MLI appears to experience an increasing trend in view of the extensive automation in industries. Multilevel inverters are mostly employed in high power systems like: mining applications as regenerative conveyor, medical purposes like MRI gradient coil driver, hydro pump storage, static synchronous compensator (STATCOM), flexible ac transmission system (FACTS), distributed generation, train traction, aerospace and renewable energy conversion(wind and photovoltaic). Now a day, low and medium power application using MLI is reported in applications like active filters because of the smooth output waveform.

Basically MLI is divided into three classes: they are neutral point clamped (NPC), flying capacitor (FC), and cascaded H-bridge (CHB). The NPC and FC requires complicated techniques to maintain its capacitor voltage in balanced state while the CHB requires more DC sources when the level is greater than five level.

Reliability is defined as "the ability of a component or a device to perform the desired function under the given conditions over a stipulated time period" and is often measured as failure probability or failure frequency. The reliability of the multilevel inverters is analyzed by scheming the mean time to failure for each component. There are basically two different methods of reliability estimation, approximate and exact method. The results of exact method and approximate method are same, and the exact values are 50,036, 42,245 and 65,451 h for NPC, FC and CHB, respectively. With adding one redundancy part at a 50,000 h period, the reliability value increased about 23.26%, 21.24%, and 24.88% for NPC, FC, and CHB, respectively [3]. Redundancy can be achieved by adding some devices in series or parallel in the conventional topologies. Salvador Ceballos proposed a system with the fault tolerant strategy of Neutral Point Clamped multilevel inverter by adding one leg (fourth leg) [4].

Sourabh Rathore and Mukhesh Kumar have explained about the different PWM techniques used for the controlling and firing of the MLI in order to compare the total harmonic distortion values for different pulse width modulation techniques [5].

In this paper, five level inverter is with an ability to tolerate a fault on switches is proposed. This fault can be classified as simple single switch failure, leg one failure, and leg two failure.

2. PROPOSED SYSTEM TOPOLOGY:

The classical Transistor clamped H-Bridge based five level inverter consists four IGBT switches and one bidirectional switch.

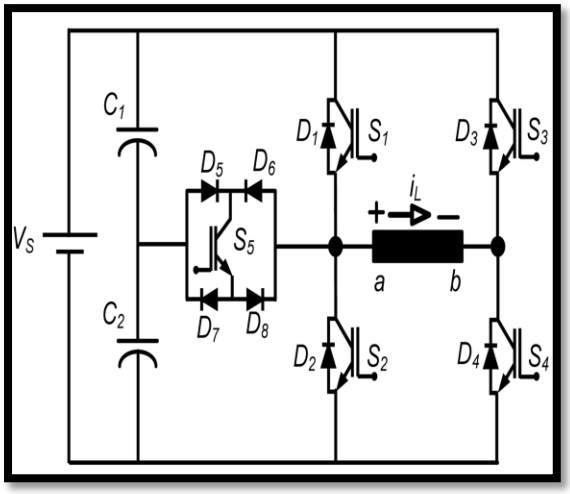


Fig 1 circuit of Classical 5 level H-Bridge inverter

Fig 1 shows the classical five level inverter circuit, here if any fault occurs to the switch then the conversion process is halted until the faulted device is replaced. This drawback is eliminated by some modification to this H-Bridge Configuration, i.e. instead of two legs of H-bridge, one leg of H-bridge (leg 1) and one leg of NPC (leg 2) is used as shown in fig 2

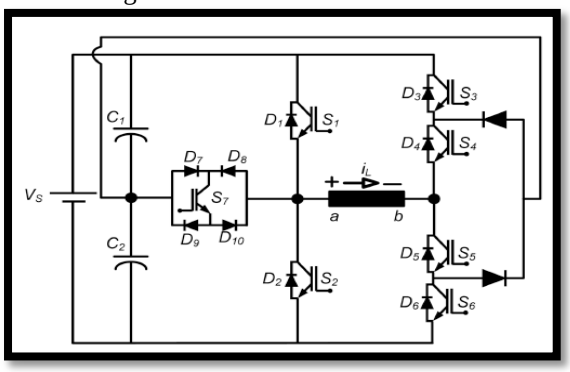


Fig 2 Modified five level transistor clamped H-bridge inverter.

This proposed system is powered by a only one DC source along with the combination of two series connected capacitors, single bidirectional switch is used, and two clamping diodes are used.

3. PWM TECHNIQUES:

Most of the power electronic converters are operated in the "switched mode". This means the switches are in either on or off state, i.e to control the flow of power in the converter. This method is called pulse width modulation (PWM), since the required average value is controlled by modulating the width of pulses. There are three different types of Multi-carries pulse width modulation.

3.1Phase disposition (PD):

The magnitude of each carrier wave is same for all carrier waves but is but is varying with time in between maximum to minimum. The frequency of the carrier wave is set at 5 kHz and reference is set at 50Hz as shown in fig 3.

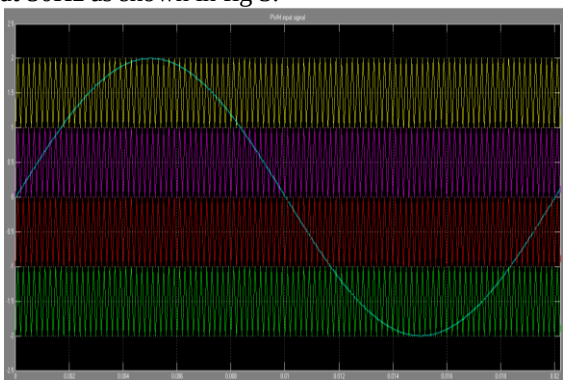


Fig 3 PD-PWM control signals

3.2 Phase Opposition Disposition PWM (PODPWM): In Phase Opposition Disposition (POD), the carrier wave is opposed to the adjacent carrier waves and carrier waves have same frequency 5 kHz, same amplitude and in phase each other as shown in fig 4.

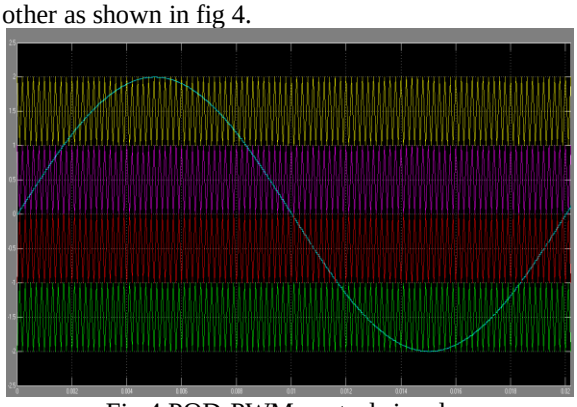


Fig 4 POD-PWM control signals

3.3 Alternate Phase Opposition Disposition PWM (APOD-PWM): In Alternate Phase Opposition Disposition PWM (APOD), all the carrier waveform have same frequency, same amplitude and but compare one carrier waveform to neighbor carrier waveform is phase shifted 180 degree.

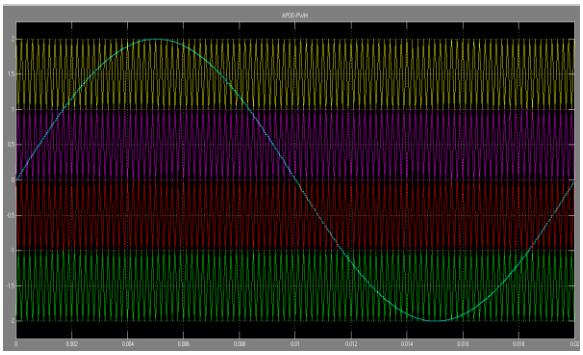


Fig 5 APOD-PWM signals

The Total Harmonic Distortion for different types of MC-PWM methods can be estimated and tabulated in successive sections.

4. SIMULATION MODELING OF PROPOSED SYSTEM:

4.1 Simulation model for control strategy under normal and fault conditions: This block consists of PWM for normal condition and also under fault condition as shown in fig 6.

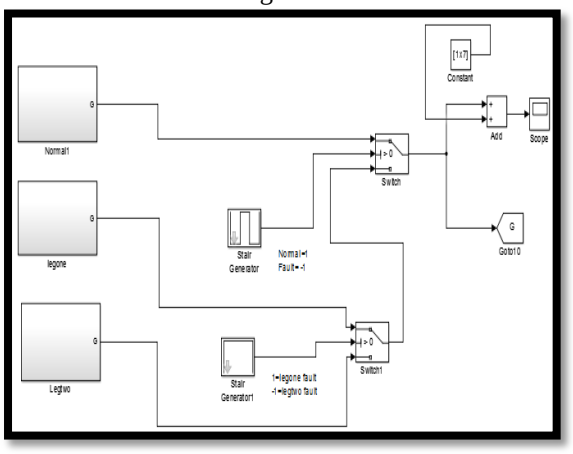


fig 6 Simulation model for control block of proposed MLI.

The entire operation depends on the stair generater and switch, the stair generator block generates a signal that changes at specified transition times. The Switch block passes through the first input or the third input depending on the value of the second input. The first and third inputs are termed as data inputs. The second input is called as control input, identify the condition under which the block passes the first input by using the condition for passing first input and threshold parameters.

4.1.1 Simulation Model for pulse generation under normal condition:

The fig 7 shows the simulation model for the PWM technique under normal condition. Pulses are generated with this model so as to operate MLIs switches.

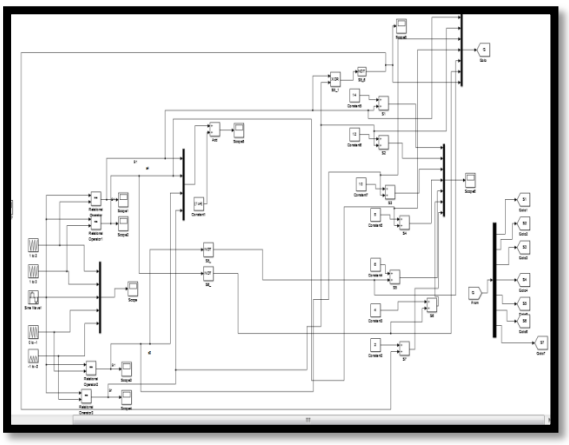


Fig 7 Simulation model for pulse generation.

The gating pulses are generated by comparison of four Carrier signals with Sinusoidal reference signal. If reference signal is greater than Carrier signal then pulse corresponding to that IGBT is turned ON. The simulated result for the control strategy model is shown in fig 8. Phase Disposition PWM method is used in our system.

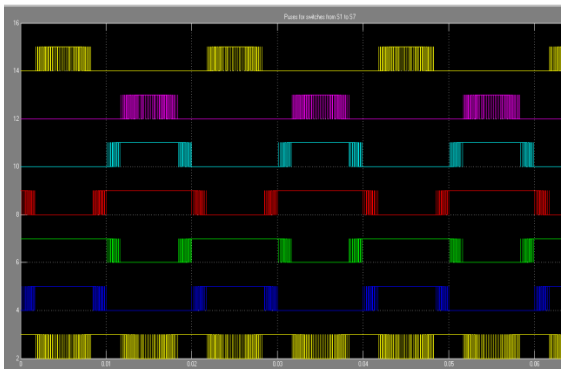


Fig 8 Gate pulses for proposed MLI

4.2 Simulation Model for Power circuit:

The fig 9 shows the simulation model of TCHB cascaded MLI, in which we can see the Output voltage and current in the scope 9. Here we will get five level output as, Vs, Vs/2, 0, -Vs, -Vs/2.

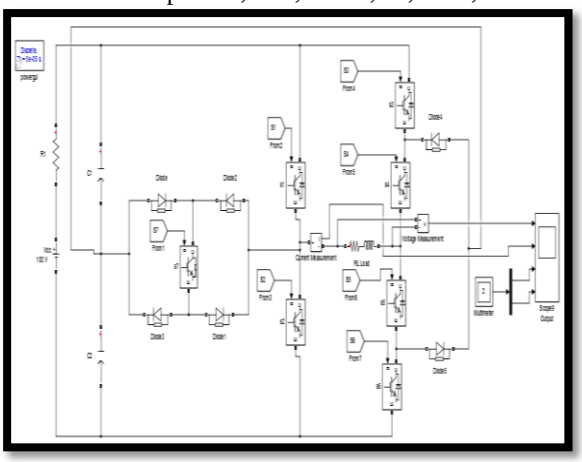


Fig 9 Simulation model TCHB cascaded MLI.

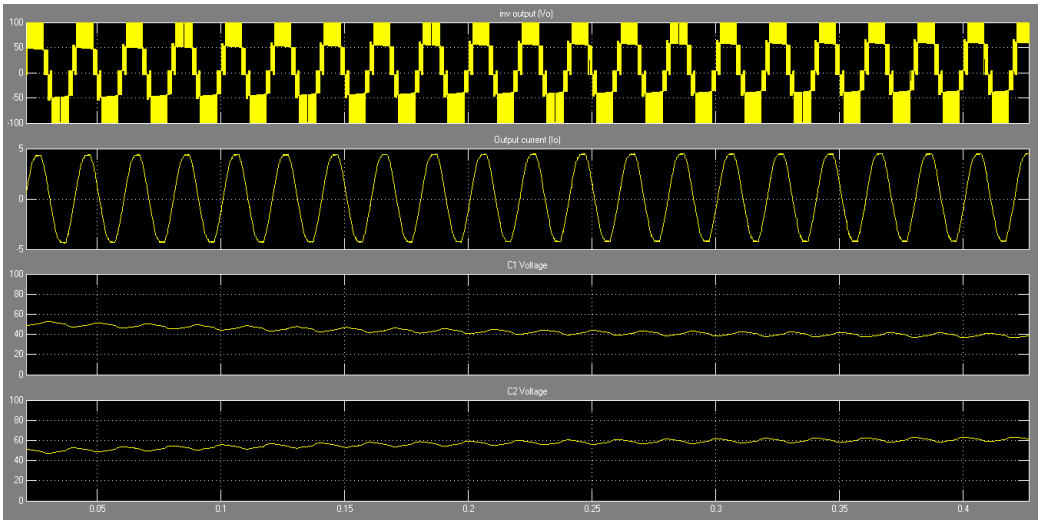
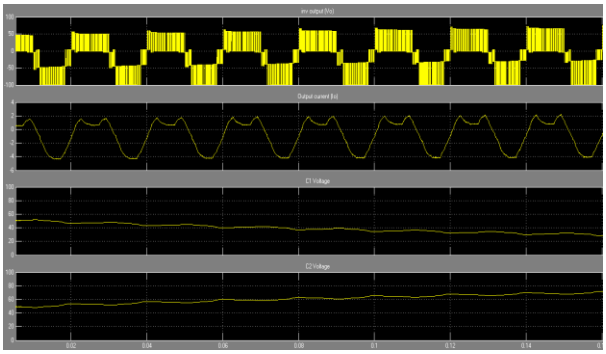


Fig 10 Simulation result for Five level Output of TCHB MLI

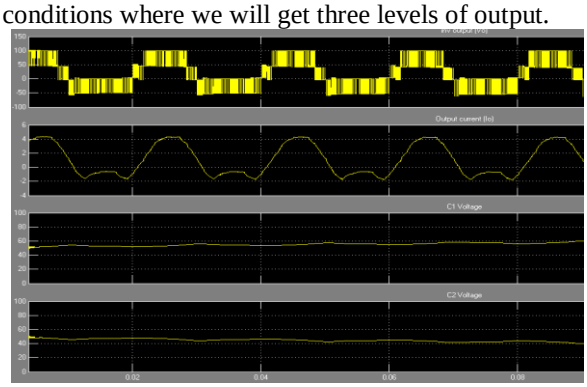
Fig 10 shows the output voltage and current for normal five level TCHB MLI. In which we can see the five levels of output voltage. We can also observe the voltage across two series connected capacitors. We can also check the capacitor voltages at every instant of time.

4.3 Simulation results for switch under fault condition:

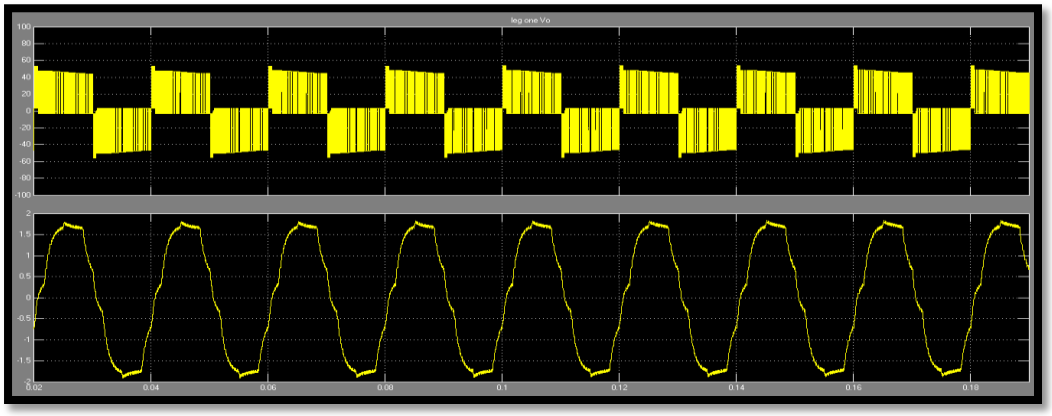
As explained in earlier section the proposed system is accomplished with the fault tolerant strategy, if any one of the switch fails means the output will not held to zero rather it gives four levels of output. The switch failure is illustrated by switch with zero gating pulse. We can also observe the leg one and leg two failure conditions where we will get three levels of output.



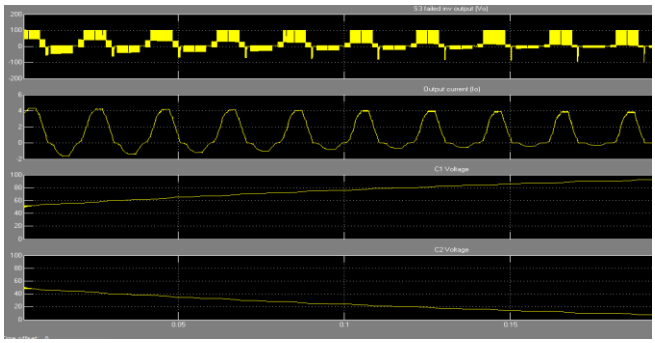
(a) Switch S1 fault



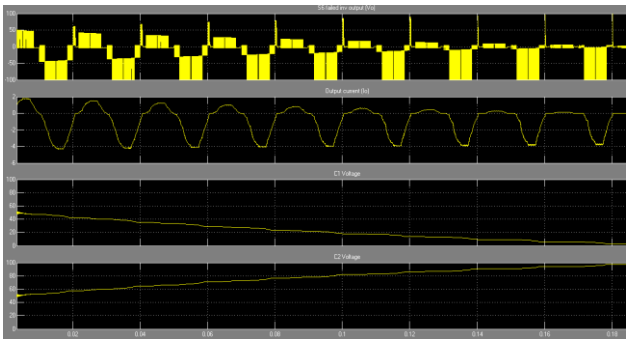
(b) Switch S2 fault



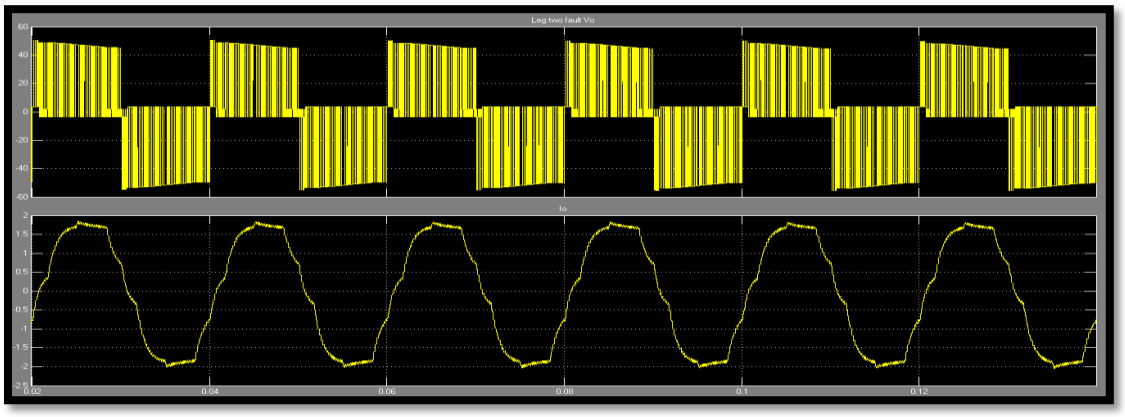
(c) Leg one fault



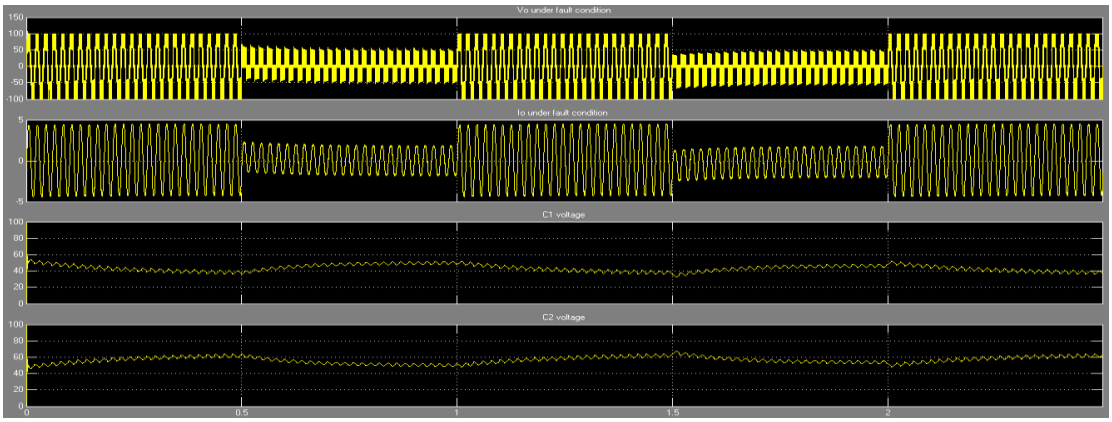
(d) Switch S3 fault



(e) Switch S6 fault



(f) Leg two fault



(g) Normal and fault condition

Fig 11 Simulation results of proposed system

4.3.1 Fault on leg one:

This leg is composed of the CHB switch configuration hence consist of two main switches S1 and S2. Fig 11*a* and *b* shows the simulation waveforms for fault on switch *S*1 and switch *S*2, respectively. Under the fault state on *S*1, the voltage of the capacitor *C*1 decreases slightly and the voltage of the capacitor *C*2 increases slightly, this drop and rise in voltages are due to the prominence of the inductor in the load. Under this condition we will get four levels of output i.e. Vs/2, 0, -Vs/2, -Vs.

Similarly when switch S2 is under fault condition, we will observe the four level output as shown in fig 11b. The voltage across capacitor *C*1 increases and the voltage across capacitor *C*2 decrease. When the fault is cleared and the control strategy is reconfigured the respective capacitor voltage again come back to half of the DC source voltage due to the self voltage balancing capability of the proposed inverter.

When both the switches are failed then we will get three levels of output as shown in fig 11c.

4.3.2 Fault on leg two:

This leg is composed of the NPC switch configuration and hence formed by four switches and two diodes which are used to clamp the blocking voltage of the switches. When a fault on *S*3 takes place, the voltage on capacitor *C*1 will get fully charged up to the supply voltage and voltage on *C*2 will get discharged to zero as shown in Fig. 11d. This happens because the path in which capacitor *C*1 discharges gets interrupted due to fault on *S*3. When the fault is cleared, the discharging of *C*1 takes place and eventually settles at half of the supply voltage.

Similar conditions are seen when the fault on *S*6 takes place, but this time, capacitor *C*1 discharges to zero and capacitor *C*2 charges to the full supply voltage as depicted in fig 11 e

Fig 11 g shows the simulation result for combined model, for time 0 to 0.5 s the system is under normal condition so we will get five level of output and the voltage across the two capacitors is balanced. For time period 0.5 to 1 s the system is under fault condition i.e. we will get three levels of output.

Hence the reliability of the proposed multilevel inverter is said to be improved, as the output is continues even under fault condition also.

4.4 Total Harmonic Distortion (THD):

Pulse Width Modulation (PWM) control techniques tries to reduce the total harmonic distortion (THD) of the output voltage. Increasing the switching frequency of the PWM pattern reduces the lower frequency harmonics by moving the switching frequency carrier harmonic and associated sideband harmonics away from the fundamental frequency component. This increased switching frequency reduces harmonics, which results in a lower THD with high quality output voltage waveforms of desired fundamental RMS value and frequency which are as close as possible to sinusoidal wave shape. Any deviation in the sinusoidal wave shape will result in harmonic currents in the load and this harmonic current produces the electromagnetic interference (EMI), harmonic losses and torque pulsation in the case of motor drives. Higher switching frequency can be employed for low and medium power inverters, whereas, for high power and medium voltage applications the switching frequency should be low. Harmonic reduction can then be strictly related to the performance of an inverter with any switching strategy.

The table 1 gives the estimation and comparision of total harmonic distortion of different PWM techniques. The simulation results of control signals are as given in section 3.

Table 1 THD Comparision for different PWM techniques

Sl.No.	**PWM Techniques**	**%Voltage THD**	**%Current THD**
01	Phase Disposition	35.11	7.0
02	Phase Opposition Disposition	34.65	6.75
03	Alternate Phase Opposition Disposition	34.41	6.60
04	Variable Frequency	28.36	6.24

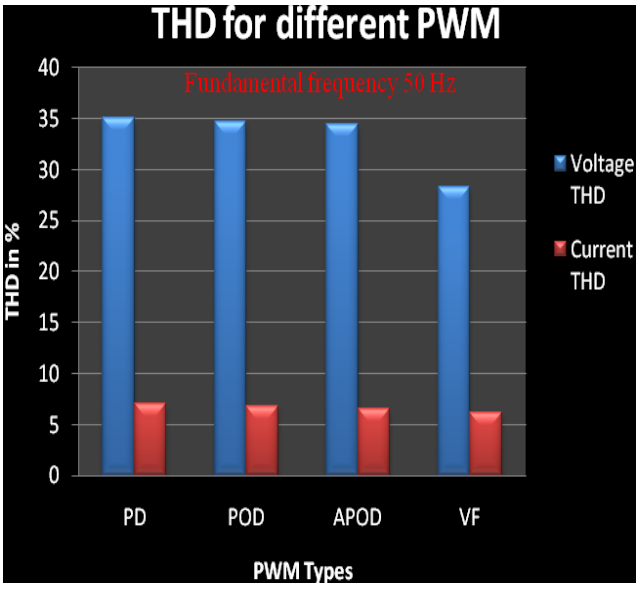


Fig 12 Voltage and Current THD for different PWM types.

The voltage and current THD is lowest for Veriable Frequency PWM as compared to other methods of

PWM techniques. And the THD is highest for Phase disposition PWM method.

5. CONCLUSION:

In this paper, the improvement in reliability of transistor clamped H-Bridge inverter is done by adding one NPC leg instead of CHB leg. The addition of NPC leg helps in creating inner voltage redundancies so that inverter can still be operated under faulty conditions as three-level inverter. The capacitor self-voltage balancing can also be achieved. The total harmonic distortion(THD) for different PWM techniques are estimated and compared. The modeling analysis and estimation is done on MATLAB software based Simulation on SIMULINK platform for five-level TCHB inverter.

REFERENCES:

[1] Shivam Prakash Gautam , Shubhrata Gupta, Lalit Kumar, 'Reliability improvement of transistor clamped H-bridge-based cascaded multilevel inverter'. IET Journals., 2017, pp.770-781

[2] Rodriguez, J., Lai, J.-S., Peng, et al. .: 'Multilevel inverters a survey of topologies, controls, and applications', *IEEE Trans. Ind. Electron.*, 2002, 49, (4), pp. 724–738

[3] Omid Alavi, Abbas Hooshmand Viki and Sadegh Shamlou.: 'A Comparative Reliability Study of Three Fundamental Multilevel Inverters Using Two Different Approaches'.

[4] Ceballos, Pou, J.,Zaragoza, J., et al.: 'Fault-tolerant neutral-point-clamped converter solutions based on including a fourth resonant leg'. IEEE Trans.Ind.Electron.,2011,58,(6), pp. 2293-2303.

[5] Lezana, P.,Aguilera, R., Rodriguez, J: 'Fault Detection on Multicell Converter Based on Output Voltage Frequency Analysis'. IEEE Trans.Ind.Electron., 2009, 56.(6), pp. 2275-2283.

[6] Sourabh Rathore, Mukhesh Kumar Kirar et al.: 'Simulation of cascaded H-Bridge multilevel inverter using PD, POD, APOD techniques'. Electrical & Computer Engineering an International journal (ECIJ) Volume 4, number 3, September 2015.

[7] C.R. Balamurugan, S.P. Natarajan et al,: 'A Review on modulation strategies of multi-level inverter'. Indonesian Journal of electrical engineering and computer science., vol. 3, No.3, September 2016, pp.681-705.

[8] Shaoyong Yang, et al.: 'An industry-Based Survey of Reliability in Power Electronic Converters' ,IEEE Trans. Ind.Appl.,2011, pp 1441-1451.

[9] Barenna, J.A.,Marroyo, L.,Vidal, M.A.R ., et al: 'Individual Voltage Balancing Strategy for PWM Cascaded H-Bridge Converter-Based STATCOM'., IEEE Trans. Ind. Electron.,2008, pp 21-29.

[10] Ceglia, G., Guzuman, V., Sanchez, C., at al,: 'A New Simplified Multilevel Inverter Topology for DC–AC Conversion', IEEE trans. Power Electron,. 2006 , pp 1311-1319.

[11] Song, W., Huang, A.Q.: 'Fault-tolerant design and control strategy for cascaded H bridge multilevel converter-based STATCOM', *IEEE Trans.Ind.Electron.*, 2010, 57, (8), pp. 2700–2708.